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In re Application of

Application Number

07/337566

Filed

4-13-1989

Paper No.

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United States Patent Application Publication No. \_\_\_\_\_, page, \_\_\_\_\_ line \_\_\_\_\_,

United States Patent Number 5999446, column \_\_\_\_\_, line, \_\_\_\_\_ or

WIPO Pub. No. \_\_\_\_\_, page \_\_\_\_\_, line \_\_\_\_\_.

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Darlene Sines

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US005999446A

## United States Patent [19]

Harari et al.

[11] Patent Number: 5,999,446

[45] Date of Patent: Dec. 7, 1999

[54] MULTI-STATE FLASH EEPROM SYSTEM WITH SELECTIVE MULTI-SECTOR ERASE

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[75] Inventors: Eliyahou Harari, Los Gatos; Robert D. Norman, San Jose; Sanjay Mehrotra, Milpitas, all of Calif.

(List continued on next page.)

[73] Assignee: SanDisk Corporation, Sunnyvale, Calif.

[21] Appl. No.: 08/999,498

[22] Filed: Dec. 29, 1997

## Related U.S. Application Data

[63] Continuation of application No. 08/407,916, Mar. 21, 1995, Pat. No. 5,719,808, which is a continuation of application No. 07/963,851, Oct. 20, 1992, Pat. No. 5,418,752, which is a division of application No. 07/347,666, Apr. 13, 1989, abandoned.

 [51] Int. Cl. G11C 16/04  
 [52] U.S. Cl. 365/185.03; 365/185.22; 365/185.11; 365/185.3; 365/185.33; 365/185.09  
 [58] Field of Search 365/185.22, 185.11, 365/185.3, 185.33, 185.03, 185.09

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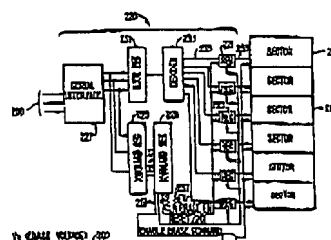
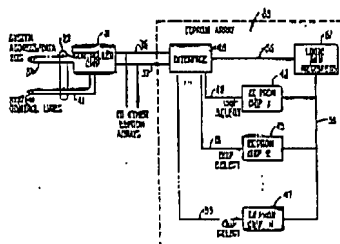
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27 Claims, 5 Drawing Sheets



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Attorney, Agent, or Firm—Majestic, Parsons, Siebert &amp; Hsue

## [57] ABSTRACT

A system of Flash EEPROM memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEPROM memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

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